IPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Tong Xiao, Robert E. Mains
Assignee:	Sun Microsystems, Inc.
Title:	Abstraction Generation for Hierarchical Timing Analysis Using Implicity Connectivity Graph Derived from Domain Propagation

Serial No.:	10/694,139	Filed:	October 27, 2003
Examiner:	Unknown	Group Art Unit:	2183
Docket No.:	SUN030009	Customer No.	33438

Austin, Texas
May 10, 2004

COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants wish to call the following documents to the attention of the Examiner.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, PO Box 1450, Alexandria, VA 22313-1450, on May 10, 2004.

Attorney for Applicant(s) — Date of Signature: 5/10/04

Respectfully submitted,

Stephen A. Terrile
Attorney for Applicant(s)
Reg. No. 32,946

U.S. Department of Commerce, Patent and Trademark Office	Attorney Docket No.	Serial No.
	SUN030009	10/694,139
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Tong Xiao et al.	
	Filing Date	Group
	October 27, 2003	2183

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AJ						☐	☐
	AK						☐	☐

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AL	Ajay J. Daga, Loa Mize, Subramanyan Sripada, Chris Wolff and Quiyang Wu "Automated Timing Model Generation" Synopsys, Inc. DAC 2002, June 2002
	AM	Noriya Kobayashi and Sharad Malik "Delay Abstraction in Combinational Logic Circuits" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, pages 1205-1212, Volume 16, Issue 10, October 1997
	AN	Clayton B. McDonald and Randal E. Bryant "A Symbolic Simulation-Based Methodology for Generating Black-Box Timing Models of Custom Macrocells" IEEE, Proceedings of the 2001 International Conference on Computer Aided Design, November 2001
	AO	S.V. Venkatesh, Robert Palermo, Mohammad Mortazavi, and Karem A. Sakallah "Timing Abstraction of Intellectual Property Blocks" IEEE 1997 Customer Integrated Circuits Conference, Pages 99-102, 1997
	AP	Hakan Yalcin, Mohammad Mortazavi, Robert Palermo, Cyrus Bamji and Karem Sakallah "Functional Timing Analysis for IP Characterization" Design Automation Conference, June 1999
	AQ	

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.